IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant on a semiconductor substrate which has gone through predetermined processes;

forming a first metal layer as a type of flat board on the dielectric layer;

forming a poly-silicon layer on the first metal layer;

patterning the poly-silicon layer and the first metal layer;

forming a second metal layer covering the patterned poly-silicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer such that the patterned poly-silicon layer is surrounded by the patterned first metal layer and the patterned second metal layer; and

patterning the second metal layer to thereby form an upper electrode constituted with the patterned second metal layer, the patterned poly-silicon layer, and the patterned first metal layer.

2. (Original) The method as recited in claim 1, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.

3. (Original) The method as recited in claim 2, wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process.

4. (Original) The method as recited in claim 3, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.

5. (Previously Presented) The method as recited in claim 1, wherein the second metal layer is constituted with one of a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.

6. (Original) The method as recited in claim 5, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000 Å.

7. (Original) The method as recited in claim 1, wherein a thickness of the poly-silicon layer ranges from about 300 Å to about 2500 Å.

8. (Previously Presented) The method as recited in claim 1, wherein the dielectric layer is constituted with one of a tantalum oxide (Ta_2O_5) layer, a titanium oxide (TiO_2) layer, an aluminum oxide (Al_2O_3)-tantalum oxide (Ta_2O_5) double layer, strontium titanium oxide ($SrTiO_3$) layer and a piezoelectric translator (PZT) layer.

9. (Previously Presented) The method as recited in claim 1, further comprising the steps of:

forming an inter-layer insulation film on the semiconductor substrate after forming the upper electrode; and

forming a contact hole exposing a portion of the upper electrode by etching the inter-layer insulation film.

10. (Currently Amended) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant on a semiconductor substrate;

forming a first metal layer as a type of flat board on the dielectric layer;

forming a poly-silicon layer on the first metal layer;

patterning the poly-silicon layer and the first metal layer;

forming a second metal layer covering the patterned poly-silicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer such that the patterned poly-silicon layer is surrounded by the patterned first metal layer and the patterned second metal layer; and

patterning the second metal layer to form an upper electrode consists of the patterned second metal layer, the patterned poly-silicon layer and the patterned first metal layer.

11. (Previously Presented) The method as recited in claim 10, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.

12. (Previously Presented) The method as recited in claim 11, wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process.

13. (Previously Presented) The method as recited in claim 12, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.

14. (Previously Presented) The method as recited in claim 10, wherein the second metal layer is constituted with one of a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.

15. (Previously Presented) The method as recited in claim 14, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000 Å.

16. (Previously Presented) The method as recited in claim 10, wherein a thickness of the poly-silicon layer ranges from about 300 Å to about 2500 Å.

17. (Previously Presented) The method as recited in claim 10, wherein the dielectric layer is constituted with one of a tantalum oxide (Ta_2O_5) layer, a titanium oxide (TiO_2) layer, an aluminum oxide (Al_2O_3)-tantalum oxide (Ta_2O_5) double layer, strontium titanium oxide ($SrTiO_3$) layer and a piezoelectric translator (PZT) layer.

18. (Previously Presented) The method as recited in claim 10, further comprising the steps of:

forming an inter-layer insulation film on the semiconductor substrate after forming the upper electrode; and

forming a contact hole exposing a portion of the upper electrode by etching the inter-layer insulation film.